

A Simple 4-Port Parasitic De-embedding Methodology for High-Frequency Characterization of SiGe HBTs

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Abstract—A new 4-port S-parameter de-embedding methodology is presented. This de-embedding technique considers distributed on-wafer parasitics in the millimeter wave band ($f > 30$ GHz). The procedure is based on simple analytical calculations and requires no equivalent circuit modeling or electromagnetic simulations. Using both EM theory and HP-ADS simulations, we show that this technique can be used to accurately extract the S-parameters to frequencies higher than 100 GHz for state-of-the-art SiGe HBTs with a maximum cutoff frequency of 180 GHz. This method is also valid for use in decoupling package parasitic

I. INTRODUCTION

For accurate evaluation of the high-frequency characteristics of state-of-the-art SiGe HBTs, extraction of the S-parameters at very high frequencies is required. The current industry paradigm is to use "open" or "open-short" standards [1][2]. Because this approach assumes lumped-component approximations, however, it begins to lose accuracy as the frequency increases above about 30 GHz. For more robust S-parameter extraction, several high-frequency de-embedding techniques have been presented [3]-[7]. These methods either use equivalent two-port analysis (with cascade, series, or parallel structures), use equivalent circuit modeling, or EM simulations. The first de-embedding type simplifies the parasitics by neglecting their insignificant components (e.g., the cascade structure neglects the parasitic feedback from the output to the input). The other types require a specific model or else simulation together with additional calibration.

As shown in [8][9], any 2-port measurement can be modeled as 4-port system which captures all of the parasitics surrounding the intrinsic device (Fig. 1). Once the 4×4 matrix of the system is solved, the intrinsic S-parameters can be accurately extracted. In the present work, we present a set of test structures that efficiently determine the Y-parameters of the 4-port parasitics network *without* equivalent circuit assumptions or EM simulations. Thus, this de-embedding methodology considers all parasitics, making it suitable for very high-frequency measurements and package parasitic decoupling.

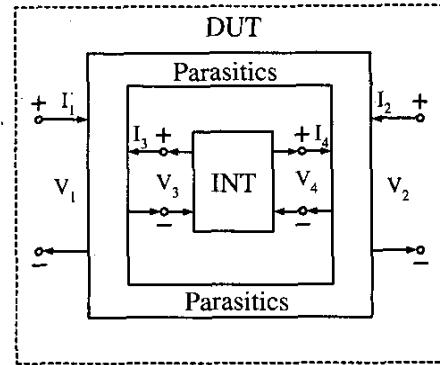


Fig. 1. Illustration of a 4-port structure. The two extrinsic ports of the device-under-test (DUT) are denoted port 1 and 2, and the two ports of intrinsic device (INT) are denoted port 3 and 4.

II. THEORY

As shown in Fig. 1, the parasitics are modeled as a 4-port system. The I-V relationships of the extrinsic and intrinsic ports can be written as a 4×4 Y-matrix according to

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} \quad (1)$$

Let V_e and I_e be the extrinsic voltage and current vectors, and V_i and I_i are the intrinsic voltage and current vectors [7]

$$\begin{pmatrix} V_e \\ V_i \end{pmatrix} = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix}$$

Thus, we have [8]

$$\begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix} \quad (2)$$

where $[Y_{ee}]$, $[Y_{ei}]$, $[Y_{ie}]$ and $[Y_{ii}]$ are four 2×2 matrices. Hence, the extrinsic Y-parameters and the intrinsic device Y-parameters

then be related by

$$\begin{aligned} Y^{DUT}V_e &= Y_{ee}V_e + Y_{ei}V_i \\ -Y^{INT}V_i &= Y_{ie}V_e + Y_{ii}V_i \end{aligned}$$

where Y^{INT} is the intrinsic device Y-parameters, and Y^{DUT} is the 2-port Y-parameters of the DUT.

Note that the current directions of the intrinsic device are opposite to the current directions of the parasitics. One thus obtains

$$Y^{DUT} = Y_{ee} - Y_{ei}(Y^{INT} + Y_{ii})^{-1}Y_{ie} \quad (3)$$

or

$$Y^{INT} = -Y_{ie}(Y^{DUT} - Y_{ee})^{-1}Y_{ei} - Y_{ii} \quad (4)$$

Once the 16 variables of the 4×4 matrix is known, one can build the appropriate 1-to-1 relationship between the extrinsic and intrinsic Y-parameters. The next step is to design test structures for determining the 4-port parameters. Since for each test structure one can measure a 2×2 Y-parameter matrix, one get four equations in each ac measurement. To solve for all 16 variables, one needs to measure at least 4 different test structures, unless approximations are made.

The industry-standard open-short de-embedding method only uses two test structures: an open and a short, together with an equivalent circuit model of this traditional open-short de-embedding method. Fig. 2 shows the equivalent circuit model of this traditional open-short de-embedding method. One can see that the distributed parasitics are simplified to one parallel capacitor (G) at the extrinsic end and two series inductors (Z) between the extrinsic and the intrinsic end. The intrinsic device Y-parameters can thus be calculated by

$$Y^{INT} = [(Y^{DUT} - Y^{OPEN})^{-1} - (Y^{SHORT} - Y^{OPEN})^{-1}]^{-1} \quad (5)$$

where $[Y^{DUT}]$, $[Y^{INT}]$, $[Y^{OPEN}]$ and $[Y^{SHORT}]$ are the Y-parameters of the DUT, the intrinsic device, the open structure, and the short structure, respectively.

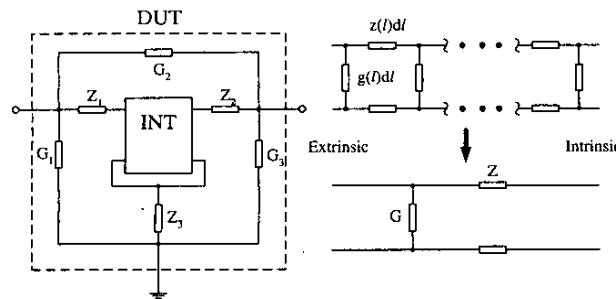


Fig. 2. Equivalent circuit model of the traditional open-short de-embedding method.

This open-short approach can be generally expressed as a simplified version of the present 4-port de-embedding technique. In the 4-port system, $V_i = 0$ for the short structure and $I_i = 0$ for the open structure. Applying these two boundary conditions to eqn. 2, one obtains

$$\begin{aligned} Y^{SHORT} &= Y_{ee} \\ Y^{OPEN} &= Y_{ee} - Y_{ei}(Y_{ii})^{-1}Y_{ie} \end{aligned}$$

It can be proven that the standard method (eqn. 5) is valid if and only if the assumption of $Y_{ei} = Y_{ie} = Y_{ii} = Y^{SHORT} - Y^{OPEN}$ is valid. At high frequency (e.g., $f > 30$ GHz), however, this assumption is no longer valid because the distributed nature of the parasitics must be considered. One direct way to solve this problem is to add more test structures for more boundary conditions in order to extract Y_{ee} , Y_{ei} , Y_{ie} and Y_{ii} . As shown below, 5 test structures can be used to extract the requisite Y matrices.

III. TEST STRUCTURES AND DE-EMBEDDING PROCEDURE

Fig. 3 shows the layout of the DUT and the needed test structures. By measuring the S-parameters of the 5 test structures and then using the simple mathematical transformations described below, one can calculate the 16 matrix variables and thus accurately de-embed the intrinsic S-parameters. The de-embedding procedure is as follows.

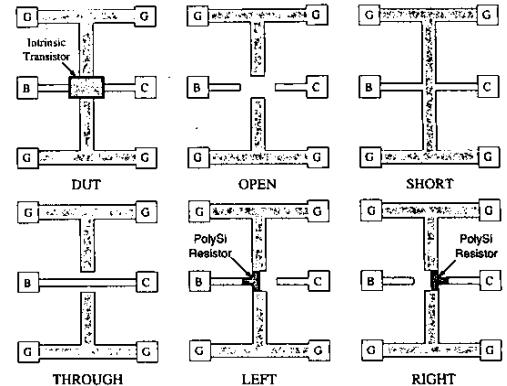


Fig. 3. The layout of the DUT and the test structures.

1) Measure the S-parameters $[S^{DUT}]$, $[S^{OPEN}]$, $[S^{SHORT}]$, $[S^{THRU}]$, $[S^{LEFT}]$ and $[S^{RIGHT}]$. Convert the S-parameters into Y-parameters.

2) Solve x and y in equations

$$|Y^{LEFT} - x[Y^{OPEN}] - (1 - x)[Y^{SHORT}]| = 0$$

$$|Y^{RIGHT} - y[Y^{OPEN}] - (1 - y)[Y^{SHORT}]| = 0$$

Note that both x and y have two solutions. For the solution $x \neq 1$ and $y \neq 1$, one can prove that

$$Y^{LEFT} - xY^{OPEN} - (1 - x)Y^{SHORT} = Y_{ei} \begin{bmatrix} 0 & 0 \\ 0 & a \end{bmatrix} Y_{ie}$$

$$Y^{RIGHT} - yY^{OPEN} - (1 - y)Y^{SHORT} = Y_{ei} \begin{bmatrix} b & 0 \\ 0 & 0 \end{bmatrix} Y_{ie}$$

where a, b are constants, and similarly

$$Y^{THRU} - Y^{SHORT} = Y_{ei} \begin{bmatrix} c & c \\ c & c \end{bmatrix} Y_{ie}$$

where c is constant.

3) Let

$$Y^{LO} = Y^{LEFT} - xY^{OPEN} - (1 - x)Y^{SHORT}$$

$$Y^{RO} = Y^{RIGHT} - yY^{OPEN} - (1 - y)Y^{SHORT}$$

$$Y^{TS} = Y^{THRU} - Y^{SHORT}$$

Obtain unscaled $[Y'_{ei}]$, $[Y'_{ie}]$ and $[Y'_{ii}]$ by using the equations below

$$Y'_{ei} = \begin{bmatrix} 1 & y_{12}^{RO}/y_{11}^{RO} \\ m_1 & m_1 y_{12}^{LO}/y_{11}^{LO} \end{bmatrix}$$

$$Y'_{ie} = \begin{bmatrix} 1 & m_2 \\ y_{21}^{RO}/y_{11}^{RO} & m_1 y_{21}^{LO}/y_{11}^{LO} \end{bmatrix}$$

$$Y'_{ii} = Y'_{ie} (Y^{SHORT} - Y^{OPEN})^{-1} Y'_{ei}$$

where

$$m_1 = \frac{y_{12}^{TS}/y_{11}^{TS} - y_{12}^{RO}/y_{11}^{RO}}{y_{12}^{LO}/y_{11}^{LO} - y_{12}^{TS}/y_{11}^{TS}}$$

$$m_2 = \frac{y_{21}^{TS}/y_{11}^{TS} - y_{21}^{RO}/y_{11}^{RO}}{y_{21}^{LO}/y_{11}^{LO} - y_{21}^{TS}/y_{11}^{TS}}$$

4) Calculate the scale factor k using the equations given below

$$k = 1/(R_I y_{11}^{LINT})$$

$$Y^{LINT} = -Y'_{ie} (Y^{LEFT} - Y^{SHORT}) Y'_{ei} - Y'_{ii}$$

where R_I is the polysilicon resistor value of the "LEFT" test structure shown in Fig. 3. Thus, the intrinsic Y-parameters are given finally by

$$Y^{INT} = -k [Y'_{ie} (Y^{DUT} - Y^{SHORT})^{-1} Y'_{ei} + Y'_{ii}] \quad (6)$$

IV. MEASUREMENT AND VERIFICATION

To compare the various de-embedding methods, the S-parameters of state-of-the-art $0.12 \times 2.5 \mu\text{m}^2$ SiGe HBTs were measured (Fig. 4).

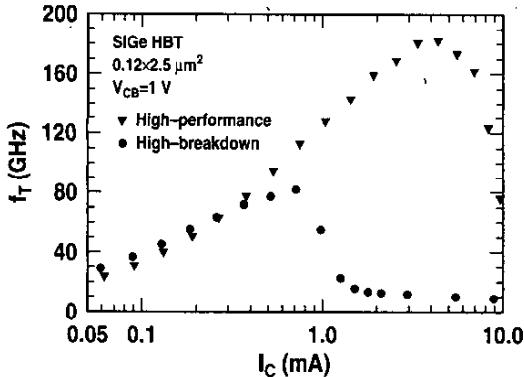


Fig. 4. Measured cutoff frequency characteristics of the state-of-the-art SiGe HBTs.

The peak f_T of these SiGe HBTs is 180 GHz at a $BV_{CEO} = 2.2$ V. The measurements were performed using a conventional microwave probing system and an HP 8510C Vector Network Analyzer over a frequency range of 4 GHz to 36 GHz.

Fig. 5 shows the measured and open-short de-embedded S-parameters. Note that for a better comparison, we have plotted $S_{21}/4$ and $S_{22} - 1$ instead of S_{21} and S_{22} . Observe that a large deviation is seen between the raw data and the de-embedded data. This is because the parasitics are comparable to the intrinsic device Y-parameters in these small devices. A more sophisticated de-embedding method is clearly required for accurate characterization of such high-speed devices.

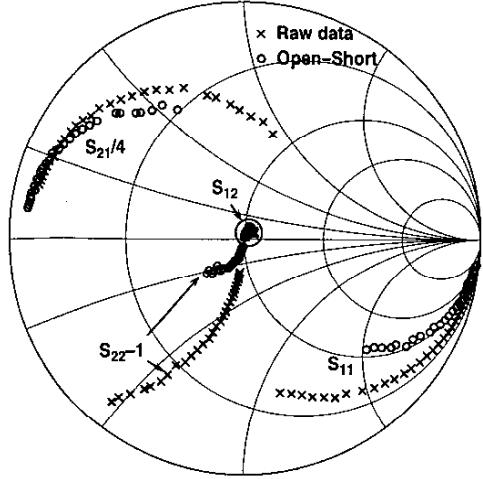


Fig. 5. Measured and de-embedded S-parameters. The device was biased at $I_C = 2$ mA and $V_{CB} = 1$ V.

To fully verify the accuracy of the proposed new 4-port de-embedding method at high frequencies, and to make a fair comparison with other de-embedding methods, one must resort to device simulations, because the (implicitly accurate) simulated intrinsic device S-parameters are needed to quantify accuracy of the various de-embedding methods. We have thus used HP-ADS with carefully calibrated device models to simulate the S-parameters of the SiGe HBTs both with and without distributed parasitics. The simulated frequency range is 1 GHz to 100 GHz. Fig. 6 shows the equivalent circuit of the DUT used in the HP-ADS simulation. A 4-port distributed parasitic system is used. The parasitics are chosen based on the measured test structure.

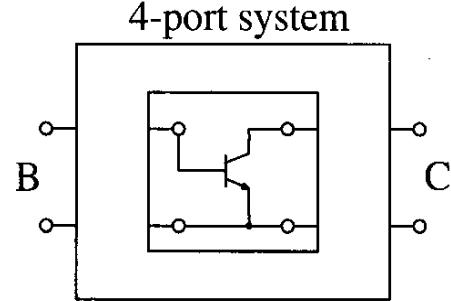


Fig. 6. The equivalent circuit of DUT used in the HP-ADS simulations.

For brevity, we show only the Y_{21} parameter for the following comparison. Fig. 7 shows the intrinsic and de-embedded Y_{21} as a function of frequency. As predicted theoretically, the open-short can be used to accurately extract the intrinsic Y-parameters at low frequency (i.e. $f < 20$ GHz). As the frequency increases, however, deviation between the open-short method and the (implicitly accurate) model results is clearly observed. By using the present 4-port de-embedding method, however, one obtains very high precision in the extracted Y-parameters, and im-

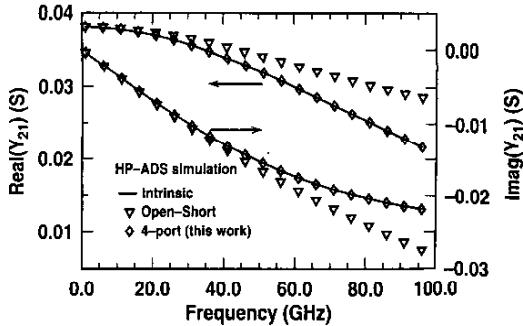


Fig. 7. The real and imaginary parts of the Y_{21} parameter as a function of frequency.

tantly, the accuracy is frequency independent.

In fact, this new method has been theoretically proven to hold for any 4-port (active/passive) parasitic system. To show this, we arbitrarily choose the 4-port Y-parameters as a parasitic system in Fig. 6, and then we extracted the Y-parameters using this present 4-port method. Fig. 8 shows the simulated intrinsic and 4-port de-embedded S-parameters. Excellent agreement is observed across the entire frequency range. In general, the present method is valid for any 4-port parasitic system, and thus would be suitable for package de-embedding, where wire-bonds, for instance, must be considered.

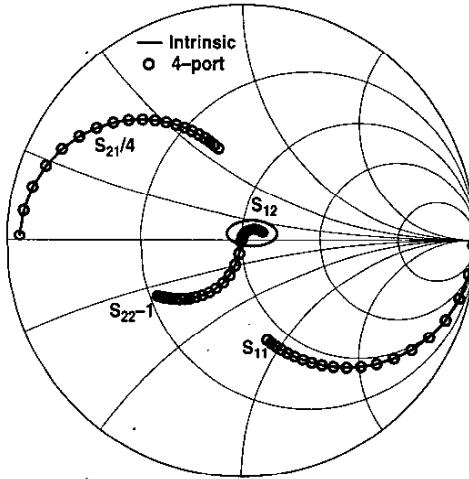


Fig. 8. Simulated intrinsic and 4-port de-embedded S-parameters. The frequency range is from 1 GHz to 100 GHz.

V. SUMMARY

We have proposed a new 4-port S-parameter de-embedding methodology which is useful for high frequency device characterization. The method requires no equivalent circuit modeling or detailed EM simulations. Based on measurements of state-of-the-art SiGe HBTs, this method is shown to be more accurate than the standard open-short method commonly used in the industry. Based on HP-ADS simulations using calibrated SiGe

HBT models, one can correctly extract S-parameters at least to 100 GHz. This method should also be useful for extracting package parasitics in complex systems.

VI. ACKNOWLEDGMENT

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